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LOW POWER 4-BIT ARITHMETIC LOGIC UNIT USING FULL-SWING GDI TECHNIQUE BASED FULL ADDER AND MULTIPLEXER

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Abstract- Power dissipation and area of the circuit are the main issues in the electronics industry, this paper provides a design of 4-Bit Arithmetic Logic Unit (ALU) using Full-Swing GDI Technique, which considered as an effective method for low power digital design by reducing the area of the circuit compared to other logic styles. The proposed ALU design consists of 2x1 Multiplexer, 4x1 Multiplexer and low power Full Adder cell to realize the arithmetic and logic operations. Simulations are performed by using MICROWIND 3.5 tool using Verilog file generated using DSCH 3.5, and implemented on CMOS 65nm technology. At first, using DSCH 3.5 tool, the circuits are implemented with full-swing GDI techniques. Simulations results validate the proposed concept and verify that full-swing GDI technique decreases the area and power used by ALU.

Keywords— Arithmetic Logic Unit (ALU); Gate Diffusion Input (GDI); Full-Swing GDI.

I. INTRODUCTION

In our daily life, we use a lot of portable electronic devices; these devices basically are low power high speed VLSI circuits that works simultaneously. One of these circuits is the Arithmetic logic unit (ALU) which considered as an essential component in many applications such as Microprocessor, digital signal processing, image processing, etc.

Addition is considered as an essential part of the arithmetic unit and almost all other arithmetic operations includes addition therefore any improvement in the adder cell is reflected as a major improvement in the ALU. In this paper a 4-Bit ALU is designed using a low power adder cell realized by the Full-Swing GDI technique and compared with previous work in terms of power dissipation and transistor count.

II. GATE DIFUSSION INPUT TECHNIQUE

GDI Technique was first proposed by Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish [1]. This technique allows implementation of various complex logic functions using only two transistors as listed in Table I. The original GDI was based on using a simple cell, as shown in Fig. 1(a).

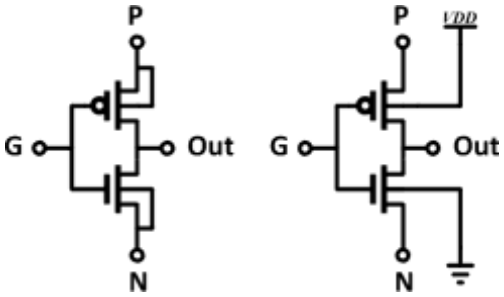

Fig. 1. GDI cell; (a) originally proposed, (b) standard CMOS compatible

However, it was proposed for fabrication in twin-well CMOS or silicon on insulator (SOI) processes, it allowed improvement in power consumption, delay and area of digital circuits compared to CMOS and PTL techniques. The drawback in GDI cell was, it suffered from reduced voltage swing due to threshold drops, which leads to performance degradation and increasing static power dissipation.

To improve the output of the GDI cells Swing restoration circuits are utilized. Morgenshtein et al. [2] proposed the Modified-GDI approach, shown in Fig. 1 (b) where the substrate terminals of NMOS and PMOS transistors connected permanently to GND and VDD, respectively. This modification enables fabrication of GDI cell in standard CMOS processes which is cost efficient compared to twin- well and SOI processes.

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TABLE I. DIFFERENT LOGIC FUNCTIONS REALIZATION USING GDI CELL.

Sr. No.	Input			Output	Function
	P	G	N		
1	B	A	0	$A\bar{B}$	F1
2	1	A	B	$A \bar{+} B$	F2
3	B	A	1	$A + B$	OR
4	0	A	B	AB	AND
5	B	A	C	$A\bar{B} + AC$	MUX
6	1	A	0	$\bar{A}$	NOT

III. ARITHMETIC LOGIC UNIT

In this paper the Full-Swing GDI technique is used to realize the circuits required to design the ALU as follows:

A. 2x1 Multiplexer

A multiplexer is a digital switch that chooses the output from several inputs based on a select signal [4], shown in Fig. 2. A 2x1 multiplexer consists of 6 transistors.

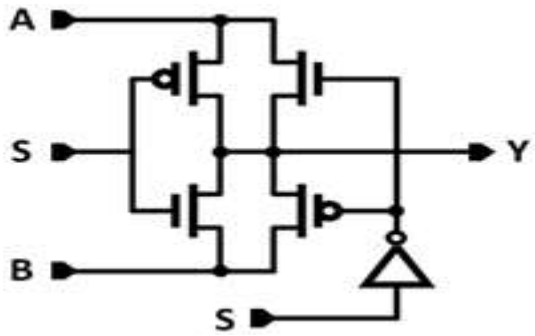

Fig. 2. Full-Swing GDI 2x1 Multiplexer

B. 4x1 Multiplexer

Using the previously discussed 2x1 multiplexer, a 4x1 multiplexer realized as shown in Fig. 3 consists only of 16 transistors.

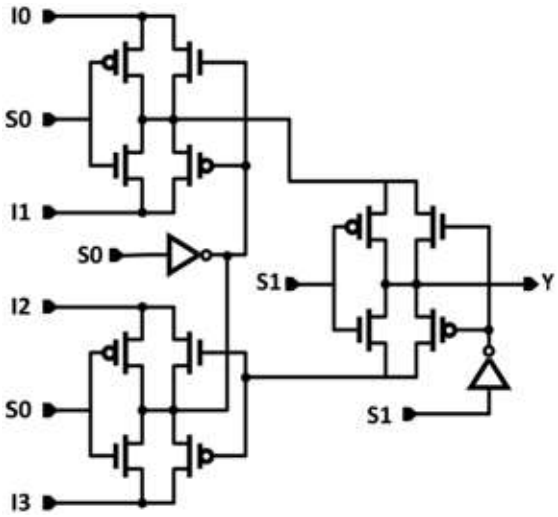

Fig. 3. Full-swing GDI 4x1 MUX

C. Full Adder

Full adder based XNOR technique has 8T, it consists of two 3T XNOR module generates the SUM output and multiplexer generates the CARRY output. Full adder is a basic component for an ALU. Depending on the three input A,B,C, the sum and carry output can be generated. Full adder based XNOR technique consumes less power. In another case when A=1 and B=0 both transistors (P1 & N1) are on and output node is discharged rapidly by N1 and N2 transistors. In this case with A=1 transistor N1 turns on which further turn on the transistor N2 and a conducting path is provided by N1 and N2. This connectivity of output node with ground discharges the output node. The switching speed of N1 is higher than N2 because delay is inversely proportional to channel width [1]. Due to on condition of transistor N1 the gate voltage of N2 increase above its threshold voltage and transistor N2 also goes in on condition. In this position the circuit is just behaving like an inverter with A=1 as input and gives output as low logic. Transistor P1 is just acting as load resistance with grounded gate input (B= 0).

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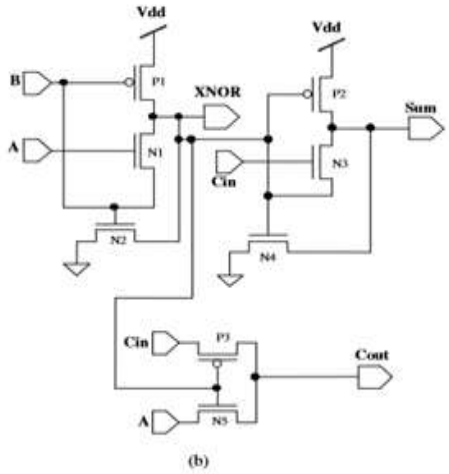

Fig. 4. Full-Swing GDI XNOR based Full Adder cell

D. Design of Arithmetic Logic Unit

An ALU is a key component in the Central Processing Unit (CPU) of any computer; even the simplest microprocessors contain one. It performs arithmetic operations such as addition, subtraction, increment, decrement and logic operations such as AND, OR, XOR and XNOR [6]. The proposed design of the 4-Bit ALU consists of 4 stages, each stage is an 1-Bit ALU realized using the previously discussed circuits as follows:

Each 1-Bit ALU stage consists of two 2x1 multiplexers, two 4x1 multiplexers and one full adder cell, this design requires 48 transistors as depicted in Fig. 5. Any desired operation can be performed based on the selection line S0, S1, S2 code; Table II summarizes the truth table of the proposed ALU.

TABLE II. TRUTH TABLE OF THE PROPOSED 4-BIT ALU.

S2	S1	S0	Operations
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBSTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	XOR
1	1	0	XNOR
1	1	1	OR

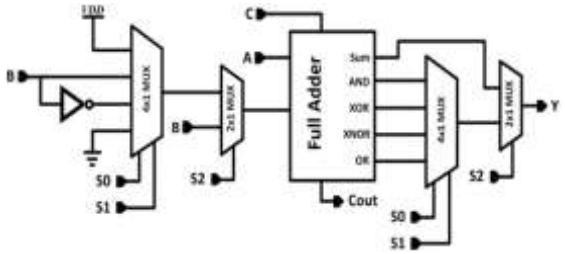

Fig. 5. Schematic of 1-Bit ALU Stage

In fig. 6, while the carry input of ALU0 connected to selection line S1 to obtain logic 1 which needed for subtraction and increment operations, however the other values don't affect the results of the logic operations.

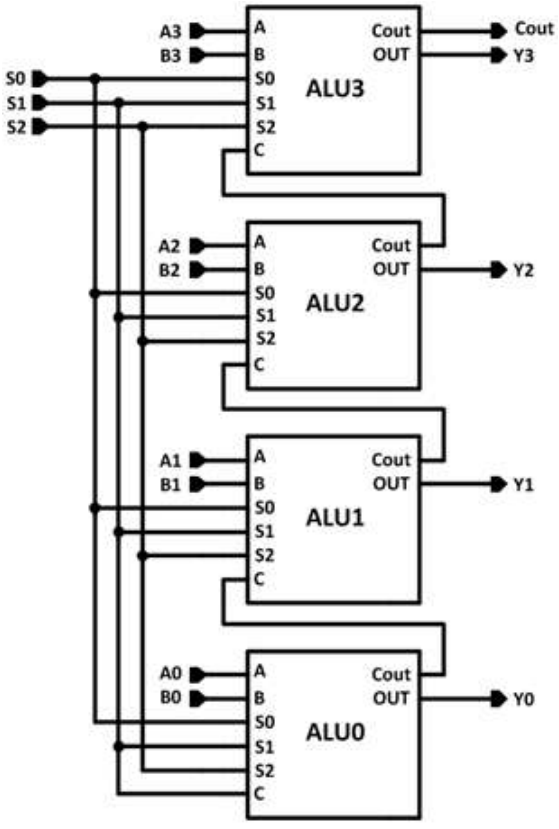

Fig. 6. Proposed 4-Bit ALU Design

IV. SIMULATION RESULTS AND COMPARISON

The proposed 4-Bit ALU circuits were designed using 65nm CMOS process in Microwind 3.5, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance. The simulations were done using

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DSCH and Microwind 3.5 with a power supply of 1V. Using A=1111, B=1010 as test inputs. Simulation results and digital schematics of some of the operations using full swing GDI technique are given below using DSCH 3.5 tool.

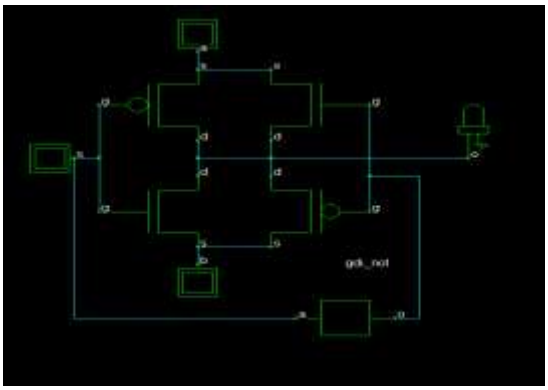

Fig. 7. Schematic of 2x1 mux designed in DSCH 3.5.

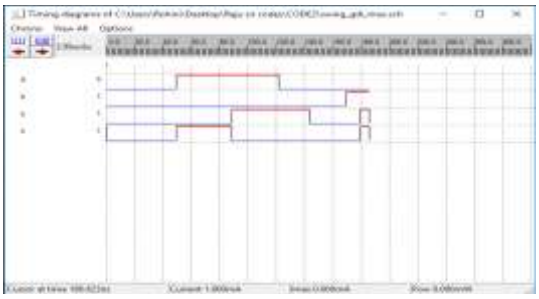

Fig. 8. Simulation output of 2x1 mux in DSCH 3.5.

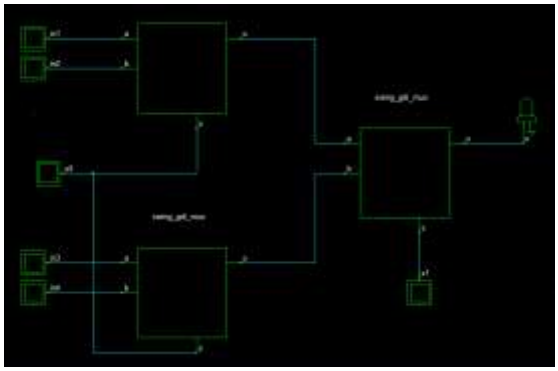

Fig. 9. Schematic of 4x1 mux designed in DSCH 3.5.

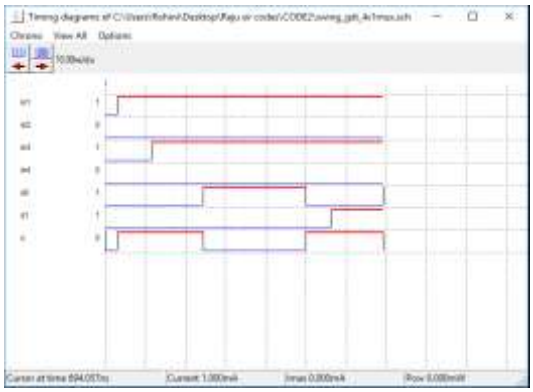

Fig. 10. Simulation result of 4x1 mux in DSCH 3.5.

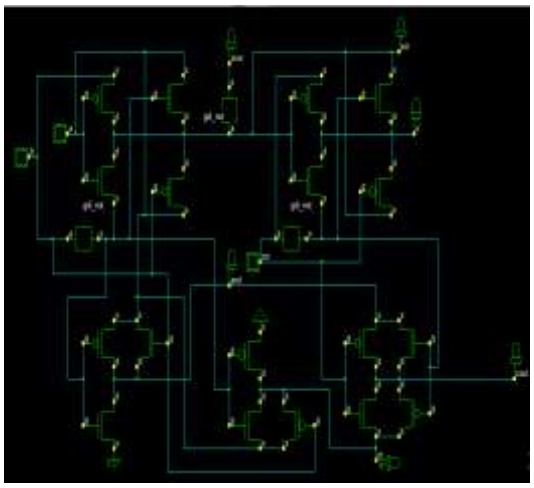

Fig. 11. Schematic of proposed full-swing GDI based full adder designed in DSCH 3.5.

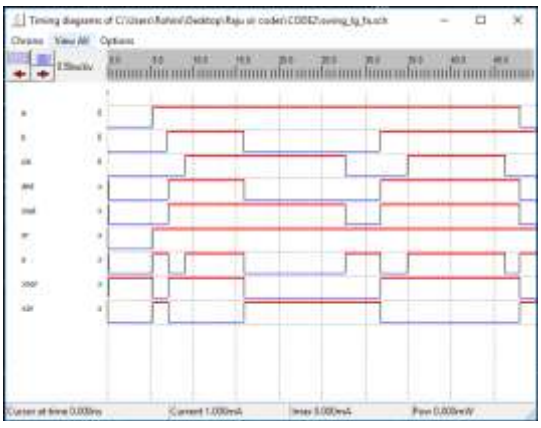

Fig. 12. Simulation result of proposed full-Swing GDI based full adder in DSCH 3.5.

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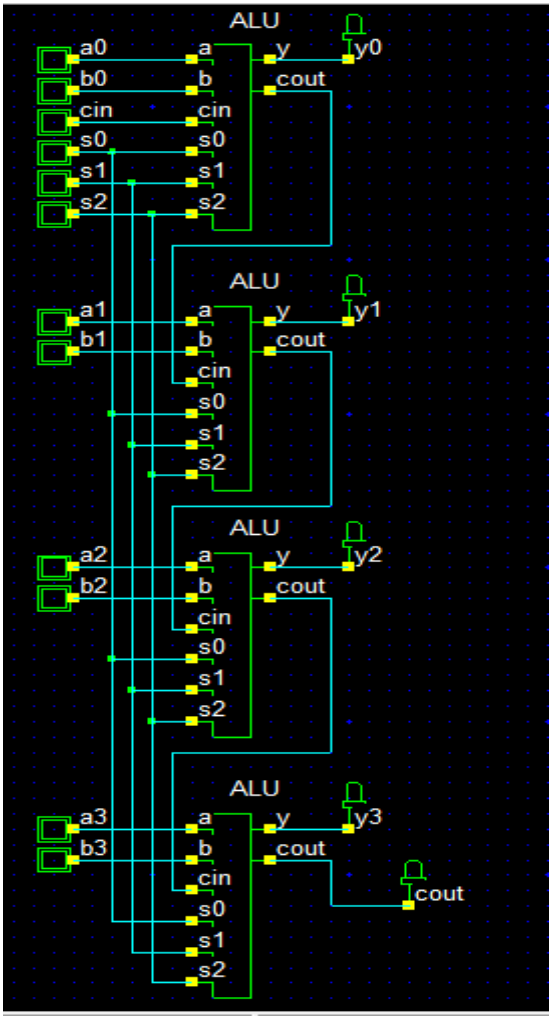

Fig. 13. Schematic of proposed full-swing GDI based ALU designed in DSCH 3.5.

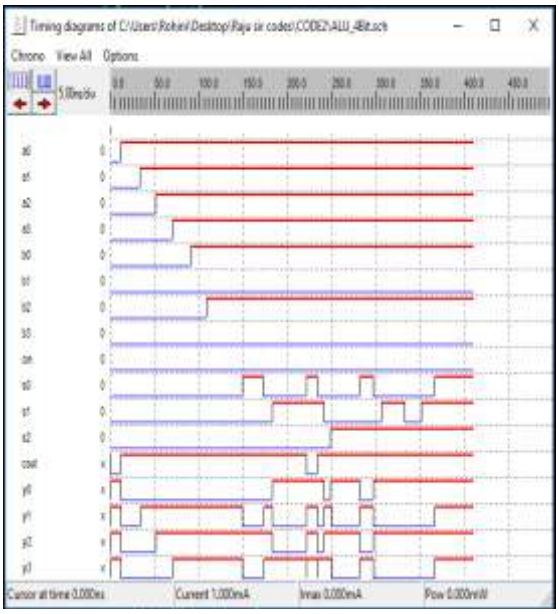

Fig. 14. Simulation result of proposed full-swing GDI based ALU in DSCH 3.5.

Fig. 16. shows the waveform of the proposed ALU. The results of the proposed design compared with the 4-Bit ALU existing design are shown in Table III.

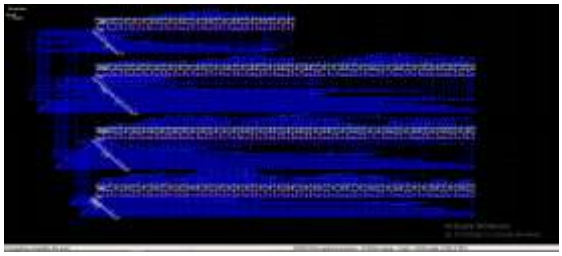

Fig. 15. Layout of proposed 4-bit ALU implemented on CMOS 65 nm technology using MICROWIND 3.5 Tool

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Fig. 16. Simulation of proposed ALU using full swing GDI in MICROWIND 3.5 Tool

Among these designs the proposed ALU design outperforms in terms of power consumption and transistor count. In respect of power consumption the proposed ALU operates at least values. Compared with the other designs the Transistor count is also reduced.

TABLE III. COMPARISION TABLE

Design	Technology	No of transistors	power	Area
Existing	65nm	324	1.850 mw	5196.3 mm2
Proposed	65nm	296	0.166 mw	3548.4 mm2

V. CONCLUSION AND FUTURE WORK

This work presents a 4-Bit ALU designed in 65nm CMOS process using the Full-Swing GDI technique and simulated using the DSCH and MICROWIND 3.5. Simulation results showed an advantage of the proposed ALU design in terms of power consumption and transistor count, while maintaining full-swing operation. The proposed design consists of transistors and operates under 1V supply voltage. In future, improvements can be done to decrease the number of transistors which results in further low power, area efficient design which has wide applications in many areas.

REFERENCES

1) A. Morgenshtein, A. Fish, and I. Wagner, “Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.

2) A. Morgenshtein, I. Shwartz, and A. Fish, “Gate Diffusion Input (GDI) logic in standard CMOS Nanoscale process,” 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2010.

3) A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Full- swing gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.

4) N. Weste, D. Harris, CMOS VLSI Design a Circuits and Systems Perspective, 4th Ed, Addison-Wesley, 2011.

5) M. Shoba, R. Nakkeeran, "GDI based full adders for energy efficient arithmetic applications", Engineering Science and Technology, an International Journal, vol. 19, no. 1, pp. 485–496, Mar. 2016.

6) Chandra Srinivasan, “Arithmetic Logic Unit (ALU) Design Using Reconfigurable CMOS Logic,” M.S. Thesis, Dept. of Electr. & Comput. Eng., Louisiana State Univ., Baton Rouge, LA, USA 2003.

7) Vivechana Dubey, Ravimohan Sairam, “An Arithmetic and Logic Unit Optimized for Area and power” IEEE Fourth International Conference on Advanced Computing & Communication Technologies.,pp.330-334, 2014.

8) G. Sree Reddy, K. V. Koteswara Rao,“32-Bit Arithmetic and Logic Unit Design With Optimized Area and Less Power Consumption By Using GDI Technique” International Journal of Research In Computer Applications and Robotics, Vol.3 Issue.4, pp. 51-66, April 2015.

9) S. Usha, M. Rajendiran, A. Kavitha, “Low Power Area Efficient ALU With Low Power Full Adder” IEEE International Conference on Computing for Sustainable Global Development (INDIACom), pp. 1500- 1505, 2016.